PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT

WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS

ABSTRACT OF THE INVENTION

A method and process reducing or eliminating electrical leakage between active areas in a semiconductor separated by isolation regions. A method and process are disclosed for the fabrication of an isolation region in a semiconductor. The method and process can be used in the fabrication of isolation regions used for the separation of adjacent active areas in an integrated circuit. A shallow trench is created on the surface of the semiconductor in regions where isolation spaces are to be formed. A layer of silicon dioxide (LINOX) is then grown over the surfaces of the trench. The LINOX covers roughened regions formed along the surfaces of the trench during its formation. The LINOX is then annealed at a temperature above the LINOX deposition temperature for a period of time. Annealing reduces stresses in the LINOX and in the surrounding semiconductor material. Annealing also increases the density of the LINOX. Thus annealing increases the LINOX resistance to gouge during subsequent processing. This leads to a reduction in dislocations in the semiconductor and a reduction in electrical leakage around the isolation region. A more robust LINOX and a reduction in electrical leakage around an isolation region allows the further shrinkage of integrated circuit dimensions. Furthermore, denuding and gettering of the semiconductor are both accomplished during the annealing step which results in a shortening of total processing time. Finally, since gouging of the LINOX no longer occurs where poly/spacer etch overlaps an active area corner, restrictions on placement of poly lines have been eliminated.